REMARKS

Claims 1-5 and 8 remain pending in the present application. The Applicants respectfully request reexamination of the present application in view of the following comments.

Allowable Matter

The Official Action indicates that Claim 5 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants thank the Examiner for indicating allowable material.

35 U.S.C. § 102

Claims 1-5 and 8 stand rejected under 35 USC § 102(b) as being allegedly unpatentable over Sakai (US 4,907,058, "Sakai"). Applicants have reviewed the cited reference and respectfully assert that embodiments in accordance with the present invention as recited in Claims 1-5 and 8 are patentable over Sakai.

With respect to Claim 1, Applicants respectfully assert that Sakai fails to teach or fairly suggest "a tile" as recited by Claim 1. While Sakai may teach some plan view elements of a semiconductor structure, Sakai is silent as to the recited tile or similar terms. Applicants respectfully assert one of ordinary skill in the art would not understand Sakai Figure 2B to teach or fairly suggest the recited "tile" for the design layout of an integrated circuit. For example, Sakai fails to teach the plan view shape of the deep n-well region 3, or of deep p-well region 2. Both deep well structures are indicated in Figure 2B with wavy lines, indicating that their design and extent are not reflected in the drawing, nor described in the related textual material. Consequently, one of ordinary skill in the art would recognize that Figure 2B does not teach or fairly suggest a "tile" for the design layout of an integrated circuit, as recited by Independent Claim 1.

For this reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, as Sakai is silent as to the recited "tile," Sakai cannot and does not teach or fairly suggest the further limitations of "a tile comprising a first layer wherein said first layer comprises a first layer element for a deep N-well pattern" or "arranging multiple instances of said tile" or "a tile array" or "merging said tiles" as recited by Claim 1. Moreover, Sakai

fails to disclose that multiple instances of Figure 2B may be "tiled" to form an array covering a portion of said integrated circuit design, as recited by Claim 1.

For these further reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 2-5 and 8 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 3, Applicants respectfully assert that Sakai fails to teach or fairly suggest "wherein said first layer element is identical in shape to said second layer element" as recited by Claim 3. Applicants respectfully assert that elements on different layers of Figure 2B, e.g., elements 5 and 8, are of different size and different shape, in contrast to this recited limitation of Claim 3.

For this additional reason, Applicants respectfully assert that Claim 3 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 4, Applicants respectfully assert that Sakai fails to teach or fairly suggest "wherein said first layer element is disposed rotated with respect to said second layer element" as recited by Claim 4. Applicants respectfully assert that Sakai is completely silent as to rotation of elements, as recited by Claim 4.

For this additional reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 8, Applicants respectfully assert that Sakai fails to teach or fairly suggest "flattening said first layer and said second layer" as recited by Claim 8. Applicants respectfully assert that Sakai is completely silent as to "flattening" layers, as recited by Claim 8.

For this additional reason, Applicants respectfully assert that Claim 8 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 1-5 and 8 stand rejected under 35 USC § 102(b) as being allegedly unpatentable over Masleid (US 7,049,699, "Masleid"). Applicants have reviewed the cited reference and respectfully assert that embodiments in

accordance with the present invention as recited in Claims 1-5 and 8 are patentable over Masleid.

Applicants respectfully note that the issue date of Masleid, May 23, 2006, post dates the priority date of the present application, February 3, 2004. As such, the cited reference does not appear to qualify as prior art under 35 USC § 102(b).

For this reason, Applicants respectfully assert that all rejections under 35 USC § 102(b) over Masleid are overcome, and respectfully solicit allowance of Claims 1-5 and 8.

In addition, with respect to Claim 1, Applicants respectfully assert that Masleid fails to teach or fairly suggest "a tile" as recited by Claim 1. In fact, Masleid fails to utilize the term "tile" or similar terms. The plan view elements illustrated, particularly the cited Figures 5A and 5B, illustrate relatively large portions of an integrated circuit. Applicants respectfully assert that one of ordinary skill in the art would not understand Figures 5A and/or 5B to teach or fairly suggest the recited "tiles."

As with the previously cited reference Williams, Masleid is directed to semiconductor structures, rather than methods of designing such structures, as

recited by Claim 1. Consequently, Masleid is completely silent as to a method of producing a design, even of producing design for embodiments of Masleid. Consequently, Masleid is absolutely silent as to the recited "tile" as recited by Claim 1.

For these additional reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, as Masleid is silent as to the recited "tile," Masleid does not teach or fairly suggest the further limitations of "a tile comprising a first layer wherein said first layer comprises a first layer element for a deep N-well pattern" or "arranging multiple instances of said tile" or "a tile array" or "merging said tiles" as recited by Claim 1. Moreover, Masleid fails to disclose that multiple instances of Figures 5A and/or 5B may be "tiled" to form an array covering a portion of said integrated circuit design, as recited by Claim 1.

For these further reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 2-5 and 8 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 2, Applicants respectfully assert that Sakai fails to teach or fairly suggest, "wherein said tile further comprises a second layer, wherein said second layer comprises a second layer element" as recited by Claim 2. Applicants respectfully assert that Figures 5A and 5B illustrate elements on a single layer only, in contrast to this recited limitation of Claim 3.

For this additional reason, Applicants respectfully assert that Claim 2 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 3, Applicants respectfully assert that Masleid fails to teach or fairly suggest, "[w]herein said first layer element is identical in shape to said second layer element" as recited by Claim 3. Applicants respectfully assert that elements of Figures 5A and 5B are of different size and different shape, in contrast to this recited limitation of Claim 3.

For this additional reason, Applicants respectfully assert that Claim 3 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 4, Applicants respectfully assert that Masleid fails to teach or fairly suggest, "[w]herein said first layer element is disposed rotated with respect to said second layer element" as recited by Claim 4. Applicants respectfully assert that Masleid is completely silent as to rotation of elements, as recited by Claim 4.

For this additional reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 8, Applicants respectfully assert that Masleid fails to teach or fairly suggest, "flattening said first layer and said second layer" as recited by Claim 8. Applicants respectfully assert that Masleid is completely silent as to "flattening" layers, as recited by Claim 8.

For this additional reason, Applicants respectfully assert that Claim 8 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

CONCLUSION

Claims 1-5 and 8 remain pending in the present application. The Applicants respectfully request reexamination of the present application in view of the remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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